IN THE CLAIMS:

Please cancel claims 40-42 and amend the remaining claims as follows:

1-21. (canceled).

22. (currently amended) A computer implemented method, comprising:

generating a netlist model for a circuit;

providing a first virtual delay element in the netlist model;

providing a first virtual clock signal to the first virtual delay element to influence a desired race resolution for the circuit; ~~and~~

providing a second virtual delay element in the netlist model;

providing a second virtual clock signal to the second virtual delay element, wherein the second virtual clock signal has different timing as compared to the first virtual clock signal; and

generating a test pattern to test the circuit in accordance with the first and second virtual clock ~~signal~~ signals for the first and second virtual delay ~~element~~ elements.

23. (previously presented) The method as recited in claim 22, further comprising:

selectively providing a virtual delay element for respective sequential elements in the circuit in accordance with respective race resolution requirements of the respective sequential elements.

24. (previously presented) The method of claim 22, wherein the virtual clock signal is identified as a primary input of an automatic test pattern generation (ATPG) system.

25. (previously presented) The method of claim 24, wherein the virtual clock signal is specified by a user of the ATPG system in accordance with a physical characteristic of the circuit.

26. (previously presented) The method of claim 25, wherein the physical characteristic comprises a delay characteristic.

27. (previously presented) The method of claim 26, wherein the delay characteristic corresponds to a length of conductive paths between circuit elements.

28. (currently amended) A system, comprising:

a processor; and

a memory coupled to the processor, the memory storing a program adapted to:

generate a netlist model for a circuit;

provide a first virtual delay element in the netlist model;

provide a first virtual clock signal to the first virtual delay element to influence a desired race resolution for the circuit; ~~and~~

provide a second virtual delay element in the netlist model;

provide a second virtual clock signal to the second virtual delay element, wherein the second virtual clock signal has different timing as compared to the first virtual clock signal; and

generate a test pattern to test the circuit in accordance with the first and second virtual clock ~~signal~~ signals for the first and second virtual delay ~~element~~ elements.

29. (previously presented) The system as recited in claim 28, wherein the program is further adapted to selectively provide a virtual delay element for respective sequential elements in the circuit in accordance with respective race resolution requirements of the respective sequential elements.

30. (previously presented) The system of claim 28, wherein the virtual clock signal is identified as a primary input of an automatic test pattern generation (ATPG) system.

31. (previously presented) The system of claim 30, wherein the virtual clock signal is specified by a user of the ATPG system in accordance with a physical characteristic of the circuit.

32. (previously presented) The system of claim 31, wherein the physical characteristic comprises a delay characteristic.

33. (previously presented) The system of claim 32, wherein the delay characteristic corresponds to a length of conductive paths between circuit elements.

34. (currently amended) A set of instructions residing in a computer readable storage medium, the set of instructions ~~being capable of execution~~ when executed by a processor ~~to~~ implement a method, the method comprising:

generating a netlist model for a circuit;

providing a first virtual delay element in the netlist model;

providing a first virtual clock signal to the first virtual delay element to influence a desired race resolution for the circuit; ~~and~~

providing a second virtual delay element in the netlist model;

providing a second virtual clock signal to the second virtual delay element, wherein the second virtual clock signal has different timing as compared to the first virtual clock signal; and

generating a test pattern to test the circuit in accordance with the first and second virtual clock ~~signal~~ signals for the first and second virtual delay ~~element~~ elements.

35. (previously presented) The set of instructions as recited in claim 34, wherein the method further comprises:

selectively providing a virtual delay element for respective sequential elements in the circuit in accordance with respective race resolution requirements of the respective sequential elements.

36. (previously presented) The set of instructions of claim 34, wherein the virtual clock signal is identified as a primary input of an automatic test pattern generation (ATPG) system.

37. (previously presented) The set of instructions of claim 36, wherein the virtual clock signal is specified by a user of the ATPG system in accordance with a physical characteristic of the circuit.

38. (previously presented) The set of instructions of claim 37, wherein the physical characteristic comprises a delay characteristic.

39. (previously presented) The set of instructions of claim 38, wherein the delay characteristic corresponds to a length of conductive paths between circuit elements.

40-42. (canceled).